

REMARKS

REQUEST TO WITHDRAW FINALITY

As indicated in the remarks to the previous response, claim 1 as previously amended was a combination of claims 1, 2, and 3, and was the same as claim 3 as already presented. More specifically, claim 1 had two additions, one of which was taken directly from claim 2, the other which was taken directly from claim 3 (which had depended on claim 2).

Previously, the examiner had rejected claim 3 as being unpatentable over Trevitt in view of Opalka. In this action, the examiner rejects claim 3 as being unpatentable over Trevitt in view of Irwin. The examiner provided a new ground of rejection to a claim (claim 3) that had not been substantially amended. Consequently, final rejection was not proper pursuant to MPEP §706.07(a).

Applicant requests that the finality of the previous action be withdrawn.

REMARKS TO AMENDMENT

As an initial matter, applicant notes that an Information Disclosure Statement was filed with the previous amendment, but an initialed PTO-1449 was not returned with the most recent official action.

Claims 1, 5-9, and 11-20 were submitted for examination. By this amendment, applicants have amended claims 1 and 8, cancelled claim 6, and added new claim 21. Reconsideration is requested.

The examiner rejected claims 1, 5, 6, 8, 9, and 11-20 as being unpatentable over Trevitt in view of Irwin; and claim 7 as being unpatentable further in view of Sakamoto.

Claim 1 has been amended to incorporate the limitations of claim 6. With respect to claim 6, the examiner states that Trevitt discloses that on any clock cycle, one memory portion is accessed for writing and on a next clock cycle the memory portion is accessed for reading. Claim 1 states, however, that “a word of data is stored into the buffer storage at the start of each clock cycle and word of data is read out of buffer storage at the end of each clock cycle. The description at col. 10, line 66 – col. 11, line 26 suggests that each cycle is a read or write, and

that the read or write cycle is alternated on even and odd cycles. Claim 1 as amended and as written in from claim 6 indicates that data is being written and read on the same clock cycle. The examiner's own statement on what Trevitt shows thus appears to conflict with what the claim language says.

Claim 8 has been amended to state that the means include "a clocked counter for incrementing a plurality of bytes, wherein on each clock signal, data is read into and read from buffer storage." As indicated above, Trevitt appears to show alternate reading and writing on consecutive clock cycles and not to perform in accordance with the claim language. In claim 8 as in claim 1, Irwin was not cited as providing such a teaching.

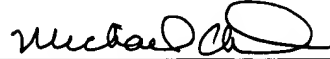
With respect to independent claim 9, it states that there is a step of "using multiple addresses to access multiple memory locations wherein only a portion of each memory location is used; and combining the data in the accessed multiple memory locations to form output data to be assigned to a single time slot." The examiner indicates that using multiple addresses to access portions of each memory location as shown at col. 10, line 66 – col. 11, line 11. From the figures, such as FIG. 8, it is not apparent where this feature is present in the description. As shown in FIG. 1 of the application, for example, the incoming word can be divided into 4 bytes, with one byte in each of a plurality of different rows of memory. Such a structure is not apparent from Trevitt.

All other claims are dependent on one of claims 1, 8, and 9, and therefore are patentable at least for the same reasons as the independent claims from which they depend.

All claims should now be in condition for allowance, and accordingly a notice for allowance is respectfully requested.

Respectfully submitted,

Date: August 19, 2004

A handwritten signature in black ink, appearing to read "Michael A. Diener", is written over a horizontal line.

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